JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech. DIGITAL SYSTEMS & COMPUTER ELECTRONICS
COURSE STRUCTURE AND SYLLABUS

I YEAR - I Semester

Code	Group	Subject	L	P	Credits
		VLSI Technology & Design	3	0	3
		Digital System Design	3	0	3
		Advanced Data Communications	3	0	3
		Microcontrollers for Embedded System Design	3	0	3
	Elective -I	Advanced Digital Signal Processing	3	0	3
		Image & Video Processing			
		Biomedical Instrumentation			
	Elective -II	CPLD & FPGA Architectures and Applications	3	0	3
		Internetworking			
		Digital Control Systems			
	Lab	Simulation Lab (VHDL/ Verilog)	0	3	2
		Seminar	-	-	2
		Total Credits (6 Theory + 1 Lab.)			22

I Year -I Sem M.Tech. (DSCE)

VLSI TECHNOLOGY & DESIGN

UNIT – I:
Review of Microelectronics and Introduction to MOS Technologies: MOS, CMOS, BiCMOS Technology, Trends and Projections.

Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: I_{ds}-V_{ds} relationships, Threshold Voltage V_t, G_m, G_{ds} and ω_o, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT – II:
LAYOUT DESIGN AND TOOLS: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

LOGIC GATES & LAYOUTS: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT – III:
COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT –IV:
SEQUENTIAL SYSTEMS: Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT – V:
FLOOR PLANNING & ARCHITECTURE DESIGN: Floor planning methods, off-chip connections, High-level synthesis, Architecture for low power, SOCs and Embedded CPUs, Architecture testing.

TEXT BOOKS:
1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A.Pucknell, 2005, PHI.
2. Modern VLSI Design - Wayne Wolf, 3rd ed., 1997, Pearson Education.

REFERENCES:
1 Principals of CMOS VLSI Design – N.H.E Weste, K.Eshraghian, 2nd ed., Adisson Wesley.

I Year -I Sem M.Tech. (DECS)

DIGITAL SYSTEM DESIGN

Unit-I: Designing with Programmable Logic Devices

Designing with Read only memories – Programmable Logic Arrays – Programmable Array logic – Sequential Programmable Logic Devices – Design with FPGA's– Using a One-hot state assignment,

State transition table- State assignment for FPGA's - Problem of Initial state assignment for One –Hot encoding - State Machine charts – Derivation of SM Charts – Realization of SM charts – Design Examples –Serial adder with Accumulator - Binary Multiplier – Signed Binary number multiplier (2's Complement multiplier) – Binary Divider – Control logic for Sequence detector – Realization with Multiplexer – PLA – PAL.

Unit-II: Fault Modeling & Test Pattern Generation

Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model

Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

Unit-III: Fault Diagnosis in Sequential Circuits

Circuit Test Approach, Transition Check Approach - State identification and fault detection experiment, Machine identification, Design of fault detection experiment.

Unit-IV: PLA Minimization and Testing

PLA Minimization – PLA folding, Fault model in PLA, Test generation and Testable PLA Design.

Unit-V: Minimization and Transformation of Sequential Machines

The Finite state Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.

Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

TEXT BOOKS:

1. Fundamentals of Logic Design – Charles H. Roth, 5th ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Logic Design Theory – N. N. Biswas, PHI

REFERENCES :

1. Switching and Finite Automata Theory – Z. Kohavi , 2nd ed., 2001, TMH
2. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.
3. Digital Circuits and Logic Design – Samuel C. Lee , PHI

I Year -I Sem M.Tech. (DECS)

ADVANCED DATA COMMUNICATIONS

Unit-I:

Digital Modulation: Introduction, Information Capacity Bits, Bit Rate, Baud, and M-ARY Coding, ASK, FSK, PSK, QAM, BPSK, QPSK, 8PSK, 16PSK, 8QAM, 16QAM, DPSK – Methods, Band Width Efficiency, Carrier Recovery, Clock Recovery.

Unit -II:

Basic Concepts of Data Communications, Interfaces and Modems: Data Communication- Components, Networks, Distributed Processing, Network Criteria- Applications, Protocols and Standards, Standards Organizations- Regulatory Agencies, Line Configuration- Point-to-point- Multipoint, Topology- Mesh- Star- Tree- Bus- Ring- Hybrid Topologies, Transmission Modes- Simplex- Half duplex- Full Duplex, Categories of Networks- LAN, MAN, WAN and Internetworking, Digital Data Transmission- Parallel and Serial, DTE- DCE Interface- Data Terminal Equipment, Data Circuit- Terminating Equipment, Standards EIA 232 Interface, Other Interface Standards, Modems- Transmission Rates.

Unit-III:

Error Detection and Correction: Types of Errors- Single- Bit Error, CRC (Cyclic Redundancy Check)- Performance, Checksum, Error Correction- Single-Bit Error Correction, Hamming Code.

Data link Control: Stop and Wait, Sliding Window Protocols.

Data Link Protocols: Asynchronous Protocols, Synchronous Protocols, Character Oriented Protocol- Binary Synchronous Communication (BSC) - BSC Frames- Data Transparency, Bit Oriented Protocols – HDLC, Link Access Protocols.

Unit-IV:

Switching: Circuit Switching- Space Division Switches- Time Division Switches- TDM Bus- Space and Time Division Switching Combinations- Public Switched Telephone Network, Packet Switching- Datagram Approach- Virtual Circuit Approach- Circuit Switched Connection Versus Virtual Circuit Connection, Message Switching.

Multiplexing: Time Division Multiplexing (TDM), Synchronous Time Division Multiplexing, Digital Hierarchy, Statistical Time Division Multiplexing.

Unit-V:

Multiple Access: Random Access, Aloha- Carrier Sense Multiple Access (CSMA)- Carrier Sense Multiple Access with Collision Detection (CSMA)- Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA), Controlled Access- Reservation- Polling- Token Passing, Channelization- Frequency- Division Multiple Access (FDMA), Time - Division Multiple Access (TDMA), - Code - Division Multiple Access (CDMA).

TEXT BOOKS:

1. Data Communication and Computer Networking - B. A.Forouzan, 3rd ed., 2008, TMH.
2. Advanced Electronic Communication Systems - W. Tomasi, 5 ed., 2008, PEI.

REFERENCES:

1. Data Communications and Computer Networks - Prakash C. Gupta, 2006, PHI.
2. Data and Computer Communications - William Stallings, 8th ed., 2007, PHI.
3. Data Communication and Tele Processing Systems - T. Housely, 2nd Edition, 2008, BSP.
4. Data Communications and Computer Networks- Brijendra Singh, 2nd ed., 2005, PHI.
5. Telecommunication System Engineering – Roger L. Freeman, 4/ed., Wiley-Interscience, John Wiley & Sons, 2004.

I Year -I Sem M.Tech. (DECS)

MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

Unit – I: Introduction to Embedded Systems
Overview of Embedded Systems, Processor Embedded into a system, Embedded Hardware Units and Devices in system, Embedded Software, Complex System Design, Design Process in Embedded System, Formalization of System Design, Classification of Embedded Systems.

Unit – II: Microcontrollers and Processor Architecture & Interfacing
8051 Architecture, Input/Output Ports and Circuits, External Memory, Counters and Timers, PIC Controllers. Interfacing Processor (8051, PIC), Memory Interfacing, I/O Devices, Memory Controller and Memory arbitration Schemes.

Unit – III: Embedded RISC Processors & Embedded System-on Chip Processor
PSOC (Programmable System-on-Chip) architectures, Continuous Timer blocks, Switched Capacitor blocks, I/O blocks, Digital blocks, Programming of PSOC, Embedded RISC Processor architecture – ARM Processor architecture, Register Set, Modes of operation and overview of Instructions

Unit – IV: Interrupts & Device Drivers
Exceptions and Interrupt handling Schemes – Context & Periods for Context Switching, Deadline & interrupt latency. Device driver using Interrupt Service Routine, Serial port Device Driver, Device drivers for Internal Programmable timing devices

Unit – V: Network Protocols
Serial communication protocols, Ethernet Protocol, SDMA, Channel & IDMA, External Bus Interface

TEXT BOOKS:

1. Embedded Systems - Architecture Programming and Design – Raj Kamal, 2nd ed., 2008,TMH.
2. PIC Microcontroller and Embedded Systems – Muhammad Ali Mazidi, Rolin D.Mckinaly, Danny Causy – PE.
3. Designers Guide to the Cypress PSOC – Robert Ashpy, 2005, Elsevier.

REFERENCES:

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.
2. ARM Systems Developers Guides- Design & Optimizing System Software - Andrew N. Sloss, Dominic Symes, Chris Wright, 2004, Elsevier.
3. Designing with PIC Microcontrollers- John B. Peatman, 1998, PH Inc.

I Year -I Sem M.Tech. (DECS)

ADVANCED DIGITAL SIGNAL PROCESSING
(ELECTIVE – I)

UNIT I

Review of DFT, FFT, IIR Filters, FIR Filters,

Multirate Signal Processing: Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design & Implementation for sampling rate conversion, Applications of Multirate Signal Processing

UNIT II

Non-Parametric methods of Power Spectral Estimation: Estimation of spectra from finite duration observation of signals, Non-parametric Methods: Bartlett, Welch & Blackman & Tukey methods, Comparison of all Non-Parametric methods

UNIT III

Parametric Methods of Power Spectrum Estimation: Autocorrelation & Its Properties, Relation between auto correlation & model parameters, AR Models - Yule-Waker & Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT –IV

Linear Prediction : Forward and Backward Linear Prediction – Forward Linear Prediction, Backward Linear Prediction, Optimum reflection coefficients for the Lattice Forward and Backward Predictors. Solution of the Normal Equations: Levinson Durbin Algorithm, Schur Algorithm. Properties of Linear Prediction Filters

UNIT V

Finite Word Length Effects: Analysis of finite word length effects in Fixed-point DSP systems – Fixed, Floating Point Arithmetic – ADC quantization noise & signal quality – Finite word length effect in IIR digital Filters – Finite word-length effects in FFT algorithms.

TEXTBOOKS:

1. Digital Signal Processing: Principles, Algorithms & Applications - J.G.Proakis & D.G.Manolokis, 4th ed., PHI.
2. Discrete Time signal processing - Alan V Oppenheim & Ronald W Schaffer, PHI.
3. DSP – A Pratical Approach – Emmanuel C.Ifeacher, Barrie. W. Jervis, 2 ed., Pearson Education.

REFERENCES:

1. Modern spectral Estimation: Theory & Application – S. M .Kay, 1988, PHI.
2. Multirate Systems and Filter Banks – P.P.Vaidyanathan – Pearson Education
3. Digital Signal Processing – S.Salivahanan, A.Vallavaraj, C.Gnanapriya, 2000,TMH

I Year -I Sem M.Tech. (DECS)

IMAGE & VIDEO PROCESSING
(ELECTIVE – I)

UNIT I Fundamentals of Image Processing and Image Transforms

Basic steps of Image Processing System Sampling and Quantization of an image – Basic relationship between pixels
Image Transforms: 2 D- Discrete Fourier Transform, Discrete Cosine Transform (DCT), Wavelet Transforms: Continuous Wavelet Transform, Discrete Wavelet Transforms.

UNIT II Image Processing Techniques

Image Enhancement
Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters.
Frequency domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, Selective filtering.
Image Segmentation
Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region Based segmentation.

UNIT III Image Compression

Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless, Huffman coding, Arithmetic coding, LZW coding, Run length coding, Bit plane coding, Transform coding, Predictive coding, Wavelet coding, JPEG Standards.

UNIT IV Basic steps of Video Processing

Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations.

UNIT V 2-D Motion Estimation

Optical flow, General Methodologies, Pixel Based Motion Esimation, Block- Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

TEXTBOOKS
1. Digital Image Processing – Gonzaleze and Woods, 3rd ed., Pearson.
2. Video processing and communication – Yao Wang, Joem Ostermann and Ya–quin Zhang. 1st Ed., PH Int.

REFERENCES :

1. Digital Video Processing – M. Tekalp, Prentice Hall International

I Year -I Sem M.Tech. (DECS)

BIO-MEDICAL INSTRUMENTATION
(ELECTIVE – I)

UNIT I

Components of Medical Instrumentation System. Bioamplifier. Static and dynamic characteristics of medical instruments. Biosignals and characteristics. Problems encountered with measurements from human beings.

UNIT II

Organisation of cell. Derivation of Nernst equation for membrane Resting Potential Generation and Propagation of Action Potential, Conduction through nerve to neuro-muscular junction.
Bio Electrodes – Biopotential Electrodes-External electrodes, Internal Electrodes. Biochemical Electrodes.

UNIT III

Mechanical function, Electrical Conduction system of the heart. Cardiac cycle. Relation between electrical and mechanical activities of the heart.

Cardiac Instrumentation Blood pressure and Blood flow measurement. Specification of ECG machine. Einthoven triangle, Standard 12-lead configurations, Interpretation of ECG waveform with respect to electro mechanical activity of the heart.

UNIT IV

Therapeutic equipment. Pacemaker, Defibrillator, Shortwave diathermy. Hemodialysis machine.
Respiratory Instrumentation Mechanism of respiration, Spirometry, Pnemuotachograph Ventilators.

UNIT V

Neuro-Muscular Instrumentation Specification of EEG and EMG machines. Electrode placement for EEG and EMG recording. Intrepretation of EEG and EMG.

TEXT BOOKS :

1. Biomedical Instrumentation and Measurements – Leslie Cromwell and F.J. Weibell, E.A. Pfeiffer, 2nd ed, 1980, PHI.
2. Medical Instrumentation, Application and Design – John G. Webster, 3rd Ed., 1998, John Wiley.

REFERENCES :

1. Principles of Applied Biomedical Instrumentation – L.A. Geoddes and L.E. Baker, 1975, John Wiley.
2. Hand-book of Biomedical Instrumentation – R.S. Khandpur, 2nd ed., 2003, TMH.
3. Biomedical Telemetry – Mackay, Stuart R1968, John Wiley.

I Year -I Sem M.Tech. (DECS)

CPLD AND FPGA ARCHITECTURE AND APPLICATIONS
(ELECTIVE – II)

UNIT –I

Programmable logic : ROM, PLA, PAL PLD, PGA – Features, programming and applications using complex programmable logic devices Altera series – Max 5000/7000 series and Altera FLEX logic-10000 series CPLD, AMD's- CPLD (Mach 1to 5), Cypres FLASH 370 Device technology, Lattice PLST's architectures – 3000 series – Speed performance and in system programmability.

UNIT – II

FPGAs: Field Programmable gate arrays- Logic blocks, routing architecture, design flow technology mapping jfor FPGAs, Case studies Xitir x XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT &T ORCA's (Optimized Reconfigurable Cell Array): ACTEL's ACT-1,2,3 and their speed performance

UNIT-III

Alternative realization for state machine chat suing microprogramming linked state machine one –hot state machine, petrinetes for state machines-basic concepts, properties, extended petrinetes for parallel controllers.

UNIT-IV

Digital front end digital design tools for FPGAs& ASICs: Using mentor graphics EDA tool ("FPGA Advantage") – Design flow using FPGAs

UNIT - V

Case studies of paraller adder cell paraller adder sequential circuits, counters, multiplexers, parellel controllers.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - S. Trimberger, Edr, 1994, Kluwer Academic Publications.
2. Field Programmable Gate Arrays, John V.Oldfield, Richard C Dore, Wiley Publications.

REFERENCES:

1. Digital Design Using Field Programmable Gate Array, P.K.Chan & S. Mourad, 1994, Prentice Hall.
2. Digital System Design using Programmable Logic Devices – Parag.K.Lala, 2003, BSP.
3. Field programmable gate array, S. Brown, R.J.Francis, J.Rose ,Z.G.Vranesic, 2007, BSP.
4. Digital Systems Design with FPGA's and CPLDs – Ian Grout, 2009, Elsevier.

I Year -I Sem M.Tech. (DECS)

INTERNETWORKING
(ELECTIVE – II)

Unit -I:

Internetworking concepts: Principles of Internetworking, Connectionless Internetworking, Application level Interconnections, Network level Interconnection, Properties of thee Internet, Internet Architecture, Wired LANS, Wireless LANs, Point-to-Point WANs, Switched WANs, Connecting Devices, TCP/IP Protocol Suite.
IP Address: Classful Addressing: Introduction, Classful Addressing, Other Issues, Sub-netting and Super-netting
IP Address: Classless Addressing: - Variable length Blocks, Sub-netting, Address Allocation. Delivery, Forwarding, and Routing of IP Packets: Delivery, Forwarding, Routing, Structure of Router.
ARP and RARP: ARP, ARP Package, RARP.

Unit -II:

Internet Protocol (IP): Datagram, Fragmentation, Options, Checksum, IP V.6.
Transmission Control Protocol (TCP): TCP Services, TCP Features, Segment, A TCP Connection, State Transition Diagram, Flow Control, Error Control, Congestion Control, TCP Times.
Stream Control Transmission Protocol (SCTP): SCTP Services, SCTP Features, Packet Format, Flow Control, Error Control, Congestion Control.
Mobile IP: Addressing, Agents, Three Phases, Inefficiency in Mobile IP.
Classical TCP Improvements: Indirect TCP, Snooping TCP, Mobile TCP, Fast Retransmit/ Fast Recovery, Transmission/ Time Out Freezing, Selective Retransmission, Transaction Oriented TCP.

Unit -III:

Unicast Routing Protocols (RIP, OSPF, and BGP: Intra and Inter-domain Routing, Distance Vector Routing, RIP, Link State Routing, OSPF, Path Vector Routing, BGP.
Multicasting and Multicast Routing Protocols: Unicast - Multicast- Broadcast, Multicast Applications, Multicast Routing, Multicast Link State Routing: MOSPF, Multicast Distance Vector: DVMRP.

Unit -IV:

Domain Name System (DNS): Name Space, Domain Name Space, Distribution of Name Space, and DNS in the internet.
Remote Login TELNET:- Concept, Network Virtual Terminal (NVT). ***File Transfer FTP and TFTP:*** File Transfer Protocol (FTP). ***Electronic Mail:*** SMTP and POP.
Network Management-SNMP: Concept, Management Components. World Wide Web- HTTP Architecture.

Unit-V:
Multimedia: Digitizing Audio and Video, Network security, security in the internet firewalls. Audio and Video Compression, Streaming Stored Audio/Video, Streaming Live Audio/Video, Real-Time Interactive Audio/Video, RTP, RTCP, Voice Over IP. Network Security, Security in the Internet, Firewalls.

TEXT BOOKS:
1. TCP/IP Protocol Suite- Behrouz A. Forouzan, Third Edition, TMH
2. Internetworking with TCP/IP Comer 3 rd edition PHI

REFERENCES:
1. High performance TCP/IP Networking- Mahbub Hassan, Raj Jain, PHI, 2005
2. Data Communications & Networking – B.A. Forouzan – 2nd Edition – TMH
3. High Speed Networks and Internets- William Stallings, Pearson Education, 2002.
4. Data and Computer Communications, William Stallings, 7th Edition., PEI.

I Year -I Sem M.Tech. (DECS)

DIGITAL CONTROL SYSTEMS

UNIT – I
SAMPLING AND RECONSTRUCTION
Introduction, Examples of Data control systems – Digital to Analog conversion and Analog to Digital conversion, sample and hold operations.

TRANSFORM ANALYSIS OF SAMPLED-DATA SYSTEMS
Introduction, Linear difference equations, pulse response, Z – transforms, Theorems of Z – Transforms, the inverse Z – transforms, Modified Z- Transforms

Z-PLANE ANALYSIS OF DISCRETE-TIME CONTROL SYSTEM
Z-Transform method for solving difference equations; Pulse transforms function, block diagram analysis of sampled – data systems, mapping between s-plane and z-plane.

UNIT – II
STATE SPACE ANALYSIS
State Space Representation of discrete time systems, Pulse Transfer Function Matrix solving discrete time state space equations, State transition matrix and it's Properties, Methods for Computation of State Transition Matrix, Discretization of continuous time state – space equations

CONTROLLABILITY AND OBSERVABILITY
Concepts of Controllability and Observability, Tests for controllability and Observability. Duality between Controllability and Observability, Controllability and Observability conditions for Pulse Transfer Function

UNIT – III
STABILITY ANALYSIS

Mapping between the S-Plane and the Z-Plane – Primary strips and Complementary Strips – Constant frequency loci, Constant damping ratio loci, Stability Analysis of closed loop systems in the Z-Plane. Jury stablility test – Stability Analysis by use of the Bilinear Transformation and Routh Stability criterion.

UNIT-IV
DESIGN OF DISCRETE TIME CONTROL SYSTEM BY CONVENTIONAL METHODS
Transient and steady – State response Analysis – Design based on the frequency response method – Bilinear Transformation and Design procedure in the w-plane, Lead, Lag and Lead-Lag compensators and digital PID controllers.

UNIT – V
STATE FEEDBACK CONTROLLERS AND OBSERVERS
Design of state feedback controller through pole placement – Necessary and sufficient conditions, Ackerman's formula.
State Observers – Full order and Reduced order observers.

TEXT BOOKS:

1. Discrete-Time Control systems - K. Ogata, Pearson Education/PHI, 2nd Edition
2. Digital Control and State Variable Methods by M.Gopal, TMH

REFERENCES:

1. Digital Control Systems, Kuo, Oxford University Press, 2nd Edition, 2003.
2. Digital Control Engineering, M.Gopal

I Year -I Sem M.Tech. (DECS)

SIMULATION LAB (VHDL/VERILOG)

CYCLE 1:

1. Simulation and Verification of Logic Gates.
2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder.
3. Simulation and verification of Decoder, MUXs, Encoder using all Modelling Styles.
4. Modelling of Flip-Flops with Synchronous and Asynchronous reset.
5. Design and simulation of Counters- Ring Counter, Johnson Counter, Up- Down Counter, Ripple Counter.
6. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in Serial out and Parallel in Parallel Out.
7. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
8. 4- Bit Multiplier, Divider.
9. ALU to Perform – ADD, SUB, AND-OR, 1'S AND 2'S COMPLIMENT, Multiplication, Division.

CYCLE 2: After Digital Circuit Description Using Verilog/ VHDL.

1. Verification of the Functionality of the circuit using function Simulators.
2. Timing Simulator for Critical Path time Calculation.
3. Syntjesis of Digital Sircuit.
4. Place and Router Techniques for FPGA's like Xilinx, Altera, Cypress, etc.,
5. Implementation of Desogn using FPGA and CPLD Devices.